2023 Digital IC Design Homework 4

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| **Simulation Result** | | | | | |
| Functional simulation | | 100 | | Gate-level simulation | 100 |
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| **Synthesis Result** | | | | | |
| Total logic elements | | | 645 | | |
| Total memory bits | | | 0 | | |
| Embedded multiplier 9-bit elements | | | 0 | | |
| Total cycle used | | | 87048 | | |
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| **Description of your design** | | | | | |
| The proposed work is implemented using a finite state machine (FSM) that is divided into ten states. The state diagram is described below:    SET\_FETCH: Sets all parameters’ initial value.  FETCH\_FAKE: Updates layer 0 index.  FETCH\_KERNEL\_IDX: Gets 3\*3 kernel’s corresponding index.  CAL: Calculates the convolutional value.  STORE\_0: Stores convolutional value to layer 0 according to layer 0 index.  SET\_FETCH\_0: Sets value to get layer 0 value.  FETCH\_0: Gets layer 0 according to layer 0 index.  FIND\_MAX: Finds the maximum value.  STORE\_1: Stores the maximum value to layer 1 according to layer 1 index.  FINISH: Finish by setting the busy signal to 0. | | | | | |

*Scoring = (Total logic elements + Total memory bits + 9\*Embedded multipliers 9-bit elements) X Total cycle used*

**\* Total logic elements must not exceed 1000.**